



HIGH POWER TRIAC**Features:**

- . All Diffused Structure
- . Same silicon wafer contains two thyristors
- . Blocking capability up to 1600 volts
- . High dv/dt Capability
- . Cold pressing encapsulation

ELECTRICAL CHARACTERISTICS AND RATINGS**Blocking-Off State**

Device Type	V _{RRM} (1)	V _{DRM} (1)	V _{RSM} (1)
BCT500E	500	500	600
BCT500M	600	600	720
BCT500N	800	800	960
BCT500P	1000	1000	1150
BCT500PB	1200	1200	1300
BCT500PD	1400	1400	1500
BCT500PM	1600	1600	1700

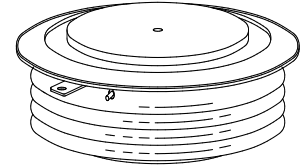
V_{RRM} = Repetitive peak reverse voltageV_{DRM} = Repetitive peak off state voltageV_{RSM} = Non Repetitive peak reverse voltage(2)

Repetitive peak reverse leakage and off state leakage	I _{RRM} / I _{DRM}	15 mA 35 mA (3)
Critical rate of voltage rise	dV/dt (4)	500 V/μsec
Critical rate of reverse voltage rise	dV/dt _{com}	500 V/μsec

Conducting-on state

Parameter	Symbol	Min.	Max.	Typ.	Units	Conditions
Average value of on-state current	I _{T(AV)}		500		A	Sinewave, 180° conduction, T _c =65°C
RMS value of on-state current	I _{TRMS}		785		A	Nominal value
Peak one cycle surge (non repetitive) current	I _{TSM}		4200		A	10.0 msec (50Hz), sinusoidal wave-shape, 180° conduction, T _j = 125 °C
I square t	I ² t		45000		A ² s	10 msec
Latching current	I _L		800		mA	V _D = 24 V; R _L = 12 ohms
Holding current	I _H		400		mA	V _D = 24 V; I = 2.5 A
Peak on-state voltage	V _{TM}		1.65		V	I _{TM} =700A
Critical rate of rise of on-state current(5,6)	di/dt		400		A/μs	Switching from V _{DRM} ≤ 1000 V, non-repetitive
Critical rate of rise of on-state current(5)	di/dt		100		A/μs	Switching from V _{DRM} ≤ 1000 V

CASE 2TA

**Notes:**All ratings are specified for T_j=25 °C unless otherwise stated.

(1) All voltage ratings are specified for an applied 50Hz/60Hz sinusoidal waveform over the temperature range -40 to +125 °C

(2) 10 msec. Max. Pulse width

(3) Maximum value for T_j=125 °C.(4) Minimum value for linear and exponential waveshape to 80% rated V_{DRM}. Gate open, T_j=125 °C

(5) Non repetitive value

(6) The value of di/dt is established in accordance with EIA/NIMA Standard RS- 397, Section5-2-2-6. The value defined would be in addition to that obtained from a snubber circuit, comprising a 0.2 μF capacitor and 20 ohms resistance in parallel with the thyristor under test.

Gating

Parameter	Symbol	Min.	Max.	Typ.	Units	Conditions
Peak gate power dissipation	P_{GM}		200		W	$t_p = 40 \mu s$
Average gate power dissipation	$P_{G(AV)}$		5		W	
Peak gate current	I_{GM}		10		A	
Gate trigger current	I_{GT}		300		mA	$V_D = 6 V; R_L = 3 \text{ ohms}; T_j = -40^\circ C$
			150		mA	$V_D = 6 V; R_L = 3 \text{ ohms}; T_j = +25^\circ C$
			125		mA	$V_D = 6 V; R_L = 3 \text{ ohms}; T_j = +125^\circ C$
Gate trigger voltage	V_{GT}		5		V	$V_D = 6 V; R_L = 3 \text{ ohms}; T_j = -40^\circ C$
			3		V	$V_D = 6 V; R_L = 3 \text{ ohms}; T_j = 0-125^\circ C$
		0.30			V	$V_D = \text{Rated } V_{DRM}; R_L = 1000 \text{ ohms}; T_j = +125^\circ C$
Peak negative voltage	V_{GRM}		5		V	

Dynamic

Parameter	Symbol	Min.	Max.	Typ.	Units	Conditions
Delay time	t_d		1.5	0.7	μs	$I_{TM} = 50 A; V_D = 67\% V_{DRM}$ Gate pulse: $V_G = 30 V; R_G = 10 \text{ ohms}; t_r = 0.1 \mu s; t_p = 20 \mu s$
Turn-off time ($V_R = -5V$)	t_q		150	100	μs	$I_{TM} > 1000 A; di/dt = 25 A/\mu s;$ $V_R \geq -5 V; \text{Re-applied } dV/dt = 200 V/\mu s \text{ linear to } 67\% V_{DRM};$ $T_j = 125^\circ C; \text{Duty cycle} \geq 0.01\%$
Reverse recovery current	I_{rr}				A	$I_{TM} > 1000 A; di/dt = 25 A/\mu s;$ $V_R \geq -50 V; T_j = 125^\circ C$

THERMAL AND MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Symbol	Min.	Max.	Typ.	Units	Conditions
Operating temperature	T_j	-40	+125		$^\circ C$	
Storage temperature	T_{stg}	-40	+150		$^\circ C$	
Thermal resistance- junction to case	$R_{\Theta(j-c)}$		0.040 0.080		$^\circ C/W$	Double sided cooled Single sided cooled
Thermal resistance - case to heatsink	$R_{\Theta(c-s)}$		0.015 0.030		$^\circ C/W$	Double sided cooled * Single sided cooled
Mounting force	P	3000 13.4	3500 15.7		lb. kN	
Weight	W			N/A	g.	

* Mounting surfaces smooth, flat and greased

